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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, QUANG N	

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,921	MILLIKEN ET AL.	
	Examiner	Art Unit	
	Quang N Nguyen	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is in response to the Amendment filed on 03/31/2005. Claims 1, 9, 16 and 21 have been amended. Claim 17 has been canceled. Claims 1-16 and 18-21 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-16 and 18-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Nataraj (US 6,757,779), herein after referred as Nataraj.

4. As to claim 1, Nataraj teaches a central processing unit (CPU), comprising:

an arithmetic logic unit *(a CAM BLOCK 1-K as illustrated in Fig. 60);*

a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations *(a CAM ARRAY 6001 containing ternary content addressable memory such as ternary CAM 404 that has rows of CAM cells 405 for storing field information, i.e., mask data M1-MX, within the CAM BLOCK 1, configured to perform classifying/filtering operations)* (Nataraj, Figs. 4 and 60, C7: L38-65, C58: L52-63 and C60:L62 – C61:L8).

5. As to claims 2-4, Nataraj teaches the CPU of claim 1, wherein the one or more matching operations includes a network packet processing operation, which includes an Internet Protocol (IP) address lookup operation (Nataraj, C16: L8-38).

6. As to claim 5, Nataraj teaches the CPU of claim 1, wherein the one or more matching operations include a packet stuff/unstuff operation (Nataraj, C14: L27-63).

7. As to claim 6, Nataraj teaches the CPU of claim 1, wherein the one or more matching operations include a packet classification operation (Nataraj, C9: L33-57).

8. As to claim 7, Nataraj teaches the CPU of claim 1, wherein the ternary content addressable memory *(the CAM ARRAT 6001)* is located within the arithmetic logic unit *(located within CAM BLOCK 1 implemented as an ALU illustrated in Fig. 60)*.

9. As to claim 8, Nataraj teaches the CPU of claim 1, further comprising:

a first register and a second register *(registers C1-C8)* configured to store a first 32-bit operand and a second 32-bit operand (Nataraj, Fig. 21 and C37: L46-62).

10. As to claim 9, Nataraj teaches the CPU of claim 8, wherein the ternary content addressable memory performs the one or more matching operations based on at least one of the first or second 32-bit operands *(TCAM array 1601 configured for x32 performs matching operations based on at least one of the first and second 32-bit operands, i.e., C1-C8)* (Nataraj, Fig. 21 and C37: L46-62).

11. As to claim 10, Nataraj teaches the CPU of claim 8, wherein the ternary content addressable memory includes a memory array including a group of 64-bit entries *(TCAM array 1601 can be configured for x32, x64, x128 or x256 operation)*, and wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand (Nataraj, C37:L15 – C38: L24).

12. As to claim 11, Nataraj teaches the CPU of claim 1, wherein the ternary content addressable memory includes a memory array that includes a group of 64-bit entries *(TCAM array 1601 can be configured for x32, x64, x128 or x256 operation)* (Nataraj, C37:L62 – C38:L24).

13. As to claim 12, Nataraj teaches the CPU of claim 11, wherein the memory array comprises 32 entries *(i.e., 32 rows)* (Nataraj, Fig. 15 and C21:L55 – C22:L45).

14. As to claim 13, Nataraj teaches the CPU of claim 1, wherein when performing the one or more matching operations, the ternary content addressable memory is configured to compare an operand to a group of entries *(the TCAM 404 is configured to compare an operand 168.69.43.100 to a group of entries 168.0.0.0/8, 168.69.0.0/16, and 168.69.62.0/24)* (Nataraj, C16:L47 – C17:L5).

15. As to claim 14, Nataraj teaches the CPU of claim 13, wherein the ternary content addressable memory is further configured to set a first flag when the operand fails to match an entry in the group of entries, and set a second flag when the operand matches multiple entries of the group of entries *(the CAM device 1200 may further include logic for generating match flag, multiple flag and/or full-flag signals)* (Nataraj, C17: L20-22).

16. As to claim 15, Nataraj teaches the CPU of claim 13, wherein prior to comparing, the ternary content addressable memory is configured to sequentially load the group of

entries from a succession of mask/value pairs transferred to the ternary content addressable memory *(the TCAM 404 is configured to sequentially load a group of entries 168.0.0.0/8, 168.69.0.0/16, and 168.69.62.0/24 as illustrated in Fig. 11)* (Nataraj, C16:L47 – C17:L5).

17. Claims 16 and 18-19 are corresponding method claims of CPU claims 1, 3 and 6; therefore, they are rejected under the same rationale.

18. Claim 20 is a corresponding system claim of method claim 16; therefore, it is rejected under the same rationale.

19. As to claim 21, Nataraj teaches an arithmetic logic unit *(a CAM BLOCK 1-K of the CAM Device 6000 as illustrated in Fig. 60)*, comprising:

a register unit *(register segments C1-C8 as illustrated in Fig. 21)*;

an operations unit *(a block flag logic unit 6007 or/and a configurable priority encoder logic unit 6005 as illustrated in Fig. 60)*; and

a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit *(a CAM ARRAY 6001 containing ternary content addressable memory such as ternary CAM 404 that has rows of CAM cells 405 for storing field information, coupled to register segments C1-C8 and to the block flag unit 6007, within the CAM BLOCK 1, configured to perform classifying/filtering operations)* (Nataraj, Figs. 4 and 60, C7: L38-65, C58: L52-63 and C60:L62 – C61:L8).

Response to Arguments

20. In the remarks, Applicant argued in substance that

(**A**) Prior Art does not teach or suggest, "an arithmetic logic unit", as claimed in the invention.

As to point (**A**), before addressing the argument, Examiner submits that the language in the quotation **"an arithmetic logic unit"** can be given a broadest and reasonable interpretation in light of the specification as *a component of a microprocessor used for arithmetic, comparative, and logical functions* (the definition of ALU from Microsoft Computer Dictionary – Fifth Edition). **Nataraj** teaches a CAM device 6000, as illustrated in Fig. 60, that includes multiple independently selectable CAM BLOCKS 1-K, wherein each of the CAM BLOCKS *(implemented as an arithmetic logic unit)* includes a configurable CAM ARRAY 6001 *(a ternary content addressable memory)*, configurable priority index table PIT 6003, configurable match flag logic and multiple match flag logic BF 6007, configurable priority encoder logic BPE 6005 and mode-responsive read/write circuitry R/W 6015 to receive read, write and compare instructions from the host processor to perform corresponding *(e.g., read, write, compare)* operations **(Nataraj, Fig. 60, C58:L52 – C59:L55 and C60:L62 – C60:L8)**.

Hence, Prior Art does teach or suggest "an arithmetic logic unit" as claimed in the invention.

(**B**) Prior Art does not teach or suggest, "a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations", as claimed in the invention.

As to point (**B**), **Nataraj** teaches a CAM ARRAY 6001 *(as illustrated in Fig. 60)* containing ternary content addressable memory such as ternary CAM 404 that has rows of CAM cells 405 for storing field information *(as illustrated in Fig. 4)*, within the CAM BLOCK 1, configured to perform classifying/filtering, read, write and compare operations as instructed by the host processor, using configurable priority index table PIT 6003, configurable match flag logic and multiple match flag logic BF 6007, configurable priority encoder logic BPE 6005 and mode-responsive read/write circuitry R/W 6015 **(Nataraj, Figs. 4 and 60, C7: L38-65, C58:L52 – C59:L55 and C60:L62 – C60:L8)**.

Hence, Prior Art does teach or suggest, "a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations", as claimed in the invention.

21. Applicant's arguments as well as request for reconsideration filed on 03/31/2005 have been fully considered but they are not deemed to be persuasive.

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Nguyen whose telephone number is (571) 272-3886.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's SPE, Rupal Dharia, can be reached at (571) 272-3880. The fax phone number for the organization is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER